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10/078,021	02/15/2002	Tsung-Han Tsai	JCLA8523	4936

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EXAMINER	
KERN, MATTHEW C	

ART UNIT	PAPER NUMBER
2654	

DATE MAILED: 02/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/078,021	TSAI ET AL.	
	Examiner	Art Unit	
	Kern Matthew	2654	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-16 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1 recites the undefined term, "cos(i,k)". The examiner has interpreted this to be a reference to $\cos(\frac{\pi}{2n}(2i+1+\frac{n}{2})(2k+1)$ for i and k=0 to n-1, p36, para 2.4.3.4.10.2, lines 4) in ISO/IEC 11172-3:1993 (E) (hereafter called ISO/IEC-3).

Claim 2 recites the ambiguous term, "efficient memory." The examiner has interpreted this to mean "modularized." Proper correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 6-9, and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai et al. ("Implementation Strategy of MPEG-2 Audio Decoder and Efficient Multi-channel Architecture" and hereafter referred as "Tsai

1") in view of Sakamoto et al. ("A fast MPEG Audio layer III algorithm for a 32-bit MCU"), and ISO/IEC-3.

As per claims 1,8, and 9, Tsai 1 teach:

- an inverse-modified discrete cosine transform(IMDCT) (IMDCT, p296, line 1)
- applying an operation of the inverse-modified discrete cosine transform to 32 sub-band samples of a compressed audio signal (32 scaled-up subband samples, audio signals, page 293, para 3, lines 6-8).

Tsai 1 and Sakamoto do not teach either IMDCT, windowing, or overlap-add for MPEG layer 3. However, ISO/IEC-3 teaches IMDCT, windowing, and overlap-add for MPEG layer III ($X_i = \sum_{k=0}^{\frac{n}{2}-1} X_k \cos(\frac{\pi}{2n}(2i+1+\frac{n}{2})(2k+1))$ for I=0 to n-1, p36, para 2.4.3.4.10.2, lines 4, windowing and n=12 for short blocks, for long blocks n=36, para 2.4.3.4.10.3, and overlapping and adding, para 2.4.3.4.10.4). It would have been obvious for one of ordinary skill at the time of invention to use Tsai's chip for the IMDCT in MPEG layer-3 so that more types of coded audio data could be decoded.

Furthermore, neither the combined method of Tsai 1 and ISO/IEC-3 standard teach using a multiplier/accumulator (MAC) for use in a dynamic windowing (DW)-IMDCT, or DWIMDCT for short, operation. However, Sakamoto

et al. teach that in order to carry out the MPEG layer-3 standard, a number of multiplications and additions per frame are needed (multiply-add operations are required, p988, col 1, para 3.1, lines1-2). Further, Tsai 1 teaches a paralleled multiplier-accumulator (MAC) between the IMDCT and IPQMF (MAC, pg 299, section 4.2, lines 10-11). Therefore, it would have been obvious for one of ordinary skill at the time of invention to arrange the MAC so as to follow the IMDCT module so that the dynamic windowing/overlapping set forth via the MPEG-layer-3 standard could be implemented and that, instead of parallelism, pipelining be used so as to reduce the amount of chip area used.

Moreover, the combined method of Tsai 1, Sakamoto et al., and ISO/IEC-3 standard does not disclose a register stack composed of registers that stores results from the DWIMDCT. However, ISO/IEC-3 specifies that for overlapping and adding with the previous block to occur, the second half of the actual block is stored to be used in the next block (p 37, heading 2.4.3.4.10.4, lines 1-2). Also, the examiner takes official notice that it is old and well-known in the art to store information on-chip via a register file so that the data can be retrieved quickly. It would have been obvious for one of ordinary skill at the time of invention to have Tsai 1's MPEG-2 audio decoder incorporate a register stack/file because it could store the large 18-bit words output of the DWIMDCT MAC0 (Multiplier accumulator) output. Further, it would have been obvious for one of ordinary skill at the time of invention to have Tsai 1's method use a register file to store the output of the IMDCT module because this result will later be used in the Dynamic

windowing step. Without the register file, the result produced by the IMDCT module would be lost, and subsequent errors in the decoding process would appear downstream. Also, a register stack could provide quick access to data, which would be important to a data-intensive application like MPEG-3 audio decoding due to the large amount of information that needs to be processed.

Finally, Tsai 1 does not teach storing the DWIMDCT result in a buffer memory. Tsai 1, however, teaches an IMDCT buffer (IMDCT Buffer, p297, figure 5). Therefore, it would have been obvious for one of ordinary skill at the time of invention to include a buffer memory in Tsai, ISO/IEC-3, and Sakamoto's datapath so that the IMDCT samples can be recalled later when dynamic windowing is applied to them. Without the buffer, the samples would be lost, and the audio decoding process could be hindered.

As per claims 6 and 14, Tsai 1, Sakamoto et al. and Tsai 2 do not teach a register stack with 18 registers. However, ISO/IEC-3 describes the process of overlapping (dynamic windowing), saying that the second half of the actual block is stored to be used in the next block. This second half is composed of 18 words (for i=0 to 17, ISO/IEC-3). It would have been obvious for one of ordinary skill at the time of invention to have Tsai 1's architecture have a register stack with 18 registers so that each of the time samples that the IMDCT module produces could be stored and later used for dynamic windowing. To have any extra registers would be wasted because this is not what the MPEG Level III standards

require. Any less, and information would be lost, thus distorting the resulting audio quality.

As per claims 7 and 15, Tsai 1 teach a post-processing stage for an architecture configured for performing the MPEG-layer II algorithm ("post-processing stage", pg 297, figure 5). However, Tsai 1 and Sakamoto et al. do not teach a post-processing part for the implementation of the MPEG-level III algorithm. It would have been obvious for one of ordinary skill at the time of invention to have Tsai 1 be modified for MPEG-layer 3 because this standard provides for higher-quality sound processing.

Further, Tsai 1 teach dividing the flowchart blocks of an algorithm and implementing the discretized part of the flow diagram into the datapath of a computer architecture (divided into two distinct stage, pre- and post-processing, p297, line 1-2, block diagram, figure 3, and overall architecture, figure 5). Also, the examiner takes official notice that it is old and well-known in the art to modularize different components on the datapath (e.g. ALU, register file, bit extender, barrel shifter, etc.) so that the design and test phase is easier.

Finally, Tsai 1 and Sakamoto et al. do not specifically teach the modules of IMDCT or synthesis filter bank module. However, the ISO/IEC-3 protocol describes these steps to implement the MPEG decoding (imdct synthesis and polyphase synthesis, figure A.4 top cartoon). It would have been further obvious to one having ordinary skill in the art at the time of invention to incorporate as two modules in Tsai 1's chip an IMDCT module and a synthesis filter bank module so

that, together, they could form the processing stage on a chip that could form the post-process portion in an audio decoding process of a Layer3 compression method in an MPEG compression standard (MP3).

As per claim 16, Tsai 1 teaches ASIC design (ASIC pg 298, para 4, line 2).

5. Claims 2-5 and 10-13 are rejected under 35 USC 103(a) as being unpatentable over Tsai 1 in view of Sakamoto and ISO/IEC-3 as applied to claims 1,8,and 9 above, and further in view of Tsai et al. (" A Novel MPEG-2 Audio Decoder with Efficient Data Arrangement and Memory Configuration", hereafter called Tsai 2.

As per claims 2 and 10, Tsai 1 teach:

- storing a plurality of data (sample are stored in IMDCT buffer, pg 298, para [4], line 11) generated by the DWIMDCT module (a output buffer of the preprocessing stage, pg 298, para [4], lines 12-13).
- providing a reading operation of a synthesis filter bank module ("input buffer of the post-processing stage" and "synthesis subband functions in the post-processing stage." , p298, para[4], lines 11-15).
- writing to and from a IMDCT buffer memory (IMDCT Buffer, figure 5, and a ping-pong mode buffer, p 298, heading 4, lines 11-14).

Tsai 1, Sakamoto and ISO-IEC-3 do not teach modularized memory layout. However, Tsai 2 teaches this concept for a synthesis window buffer (efficient data arrangement and memory configuration (para [VI] heading, pg 602). Therefore, it would have been obvious for one of ordinary skill at the time of invention to have Tsai 1's DWIMDCT buffer memory be organized in a similar fashion so that information corresponding to the sub-bands for the MPEG layer-3 algorithm can be similarly organized. This logical design could serve in bookkeeping purposes during both the design and testing phases of the chip.

As per claims 3 and 11, Tsai 1 teach pipelining between an IMDCT module and a IPQMF module in a Synthesis Subband filter module for MPEG layer 2 chip (IMDCT/IPQMF, p297, figure 5 and two-stage pipelined, pg 300, figure7). Tsai 1, Sakamoto et al., and ISO/IEC-3 do not teach a DWIMDCT module separately implemented in a manner of a pipelined process with a Synthesis filter bank module. However, Tsai 2 places a module that outputs data used as input to another distinct module close to one another (divided into two distinct stages, p297,lines 1-3) in order to speed processing and reduce cross-talk between interconnects. Furthermore, it is old and well-known in the art to speed up data transfer using the concept of pipelining. Additionally, the MPEG-layer 3 standard utilizes IMDCT and sub-band coding techniques (IMDCT, overlap-add and polyphase filterbank, figures A.3 and A.4). With all this in mind, it would have been obvious for one of ordinary skill at the time of invention to not only modularize the DWIMDCT module and Synthesis Subband filter module, the

major components of which are used to process data according to the MPEG-layer 3 algorithm, but to enable pipelining between them so as to speed up data transfer.

As per claims 4 and 12, Tsai 2 teach a memory configuration for synthesis window buffer memory comprising 5 memory banks, each of the memory banks is further divided into 32 sub-band blocks, and each of the sub-band blocks is able to store 16 sample data. Tsai 1, Sakamoto et al., and Tsai 2 do not teach DWIMDCT buffer memory of 3 memory banks, each of the memory banks divided into 32 sub-band blocks, and each of the sub-band blocks is able to store 18 sample data. However, ISO/IEC-3 states that the output of the overlap-add consists of 18 time samples for each of the 32 polyphase subbands. Also, the examiner takes Official Notice that it is old and well-known in the art to allocate as much hardware (ie memory) as is needed so that a particular algorithm can be implemented. Since the MPEG layer 3 standard dictates the highest index is 575 (thus total number of words is 576), and each word has 18 bits, that means 32 words should be used. Therefore, it would have been obvious for one of ordinary skill at the time of invention to include DWIMDCT buffer memory composed of banks each with 32 words, each word composed of 18 bits.

Furthermore, the examiner takes Official Notice that it is old and well-known in the art to choose the number of buffer memory blocks so that, if pipelining is chosen to be implemented, a proper number of buffer memory

blocks is chosen so that hazards (ie structural) when reading/writing data to the buffer do not happen. Additionally, the examiner takes Official notice that a designer will not add any more blocks than necessary, lest slowing down processing speed, increasing the chip's area, and making layout more difficult. Therefore, it would have been obvious for one of ordinary skill at the time of invention to gravitate towards 3 buffer blocks because this is the number that timing diagrams would predict to allow no structural hazards to occur while still minimizing the size of the buffer memory.

As per claims 5 and 13, Tsai 1 teaches:

- writing of the IMDCT buffer (samples stored in IMDCT buffer, p298, lines 11-13).
- reading of the IMDCT buffer by the post processing (ie synthesis subband module)("input buffer of the post-processing stage" and "synthesis subband functions in post-processing stage", pg 298, para [4], lines 11-15).

Tsai 1, Sakamoto, and ISO/IEC-3 do not teach accessing the IMDCT buffer in a specific sequence. However, Tsai 2 teach accessing data from a synthesis buffer window in a precise sequence (pg 601, figure 9). Therefore, it would have been obvious for one of ordinary skill at the time of invention to have Tsai 1 IMDCT buffer have data read/written in the same way as the synthesis buffer memory of Tsai 2 so that pipelining could be implemented and structural hazards could be avoided.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Dieffenderfer et al. (US Patent no. 5,224,213) teach a ping-pong data buffer that has read/write capability with busses of different sizes.

Chen et al. (US Patent 6,166,663) describe the architecture for MPEG-2 audio processing.

Cheng (US patent application publication 2002/0106020) teach a fast method of computing the IMDCT in audio coding.

Tsai et al. ("An MPEG Audio Decoder chip") teach a MPEG chip with IMDCT function with its result stored in RAM memory, not a register file/stack.

6. Any inquiry concerning this communication should be directed to Mr. Matthew Kern, whose telephone number is (703) 305-4828 or fax number (703) 305-9508. The examiner can normally be reached Mondays-Fridays from 9:30 am to 6 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Talivaldis Smits, can be reached at (703) 306-3011. The facsimile phone number for this Technology Center is (703) 305-9508.

Any inquiry of a general nature of relating to the status of this application should be directed to the Technology Center 2600 receptionist, whose telephone number is (703) 746-6055.

1/31/05

MCK

RICHEMOND DORVIL
SUPERVISORY PATENT EXAMINER